



#294  
1/33/04  
RESPONSE UNDER 37. CFR 1.116  
EXPEDITED PROCEDURE  
EXAMINING GROUP 2634.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of : **Confirmation No. 6208**  
Mitsuaki OSHIMA et al. : Docket No. 2000\_1391  
Serial No. 09/680,177 : Group Art Unit 2634  
Filed October 5, 2000 : Examiner A. Le  
COMMUNICATION SYSTEM :

THE COMMISSIONER IS AUTHORIZED  
TO CHARGE ANY DEFICIENCY IN THE  
FEES FOR THIS PAPER TO DEPOSIT  
ACCOUNT NO. 23-0975

**LETTER RE PROPOSED DRAWING AMENDMENTS RECEIVED**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

JAN 15 2004

Technology Center 2600

Sir:

Enclosed herewith is a photocopy of Figs. 2, 10, 17, 29, 48, 65, 67, 93, 112, 131, 138, 144, and 169 marked in red to indicate proposed drawing amendments thereto.

The Examiner is requested to approve such proposed drawing amendments. Formal drawings incorporating such amendments are filed herewith.

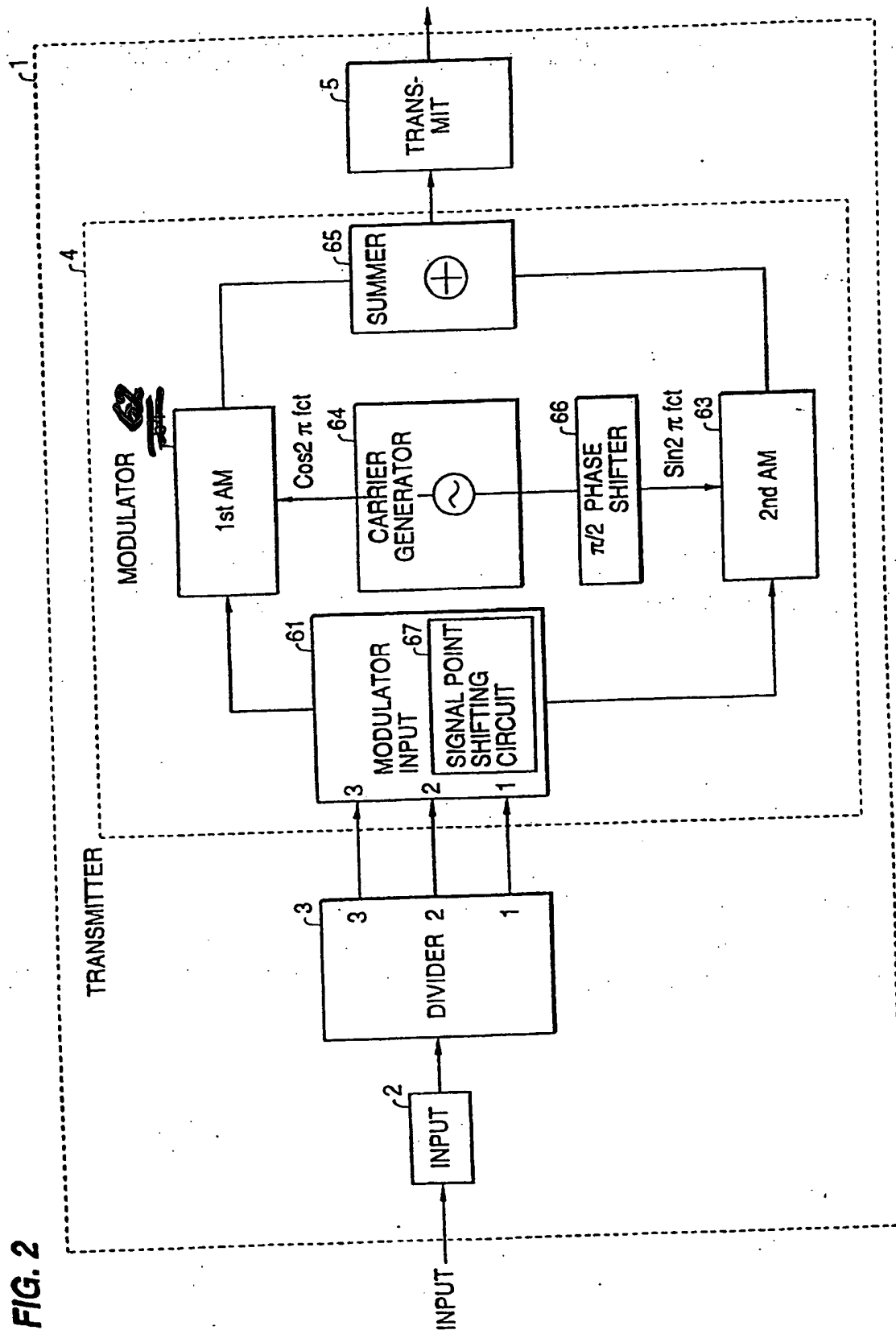
Respectfully submitted,

Mitsuaki OSHIMA et al.

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January 12, 2004



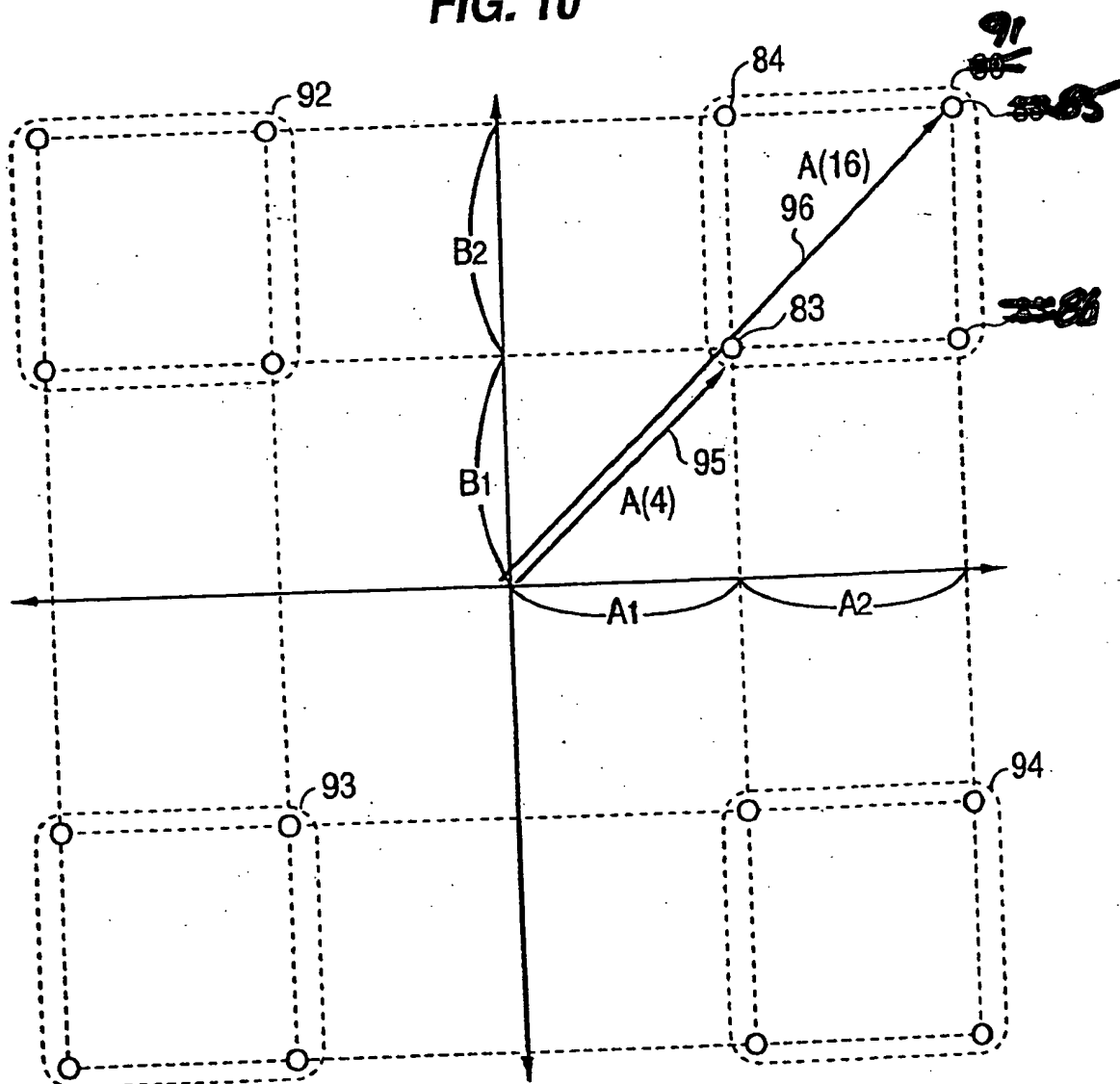


**Feb. 4, 1997**

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**5,600,672**

**FIG. 10**



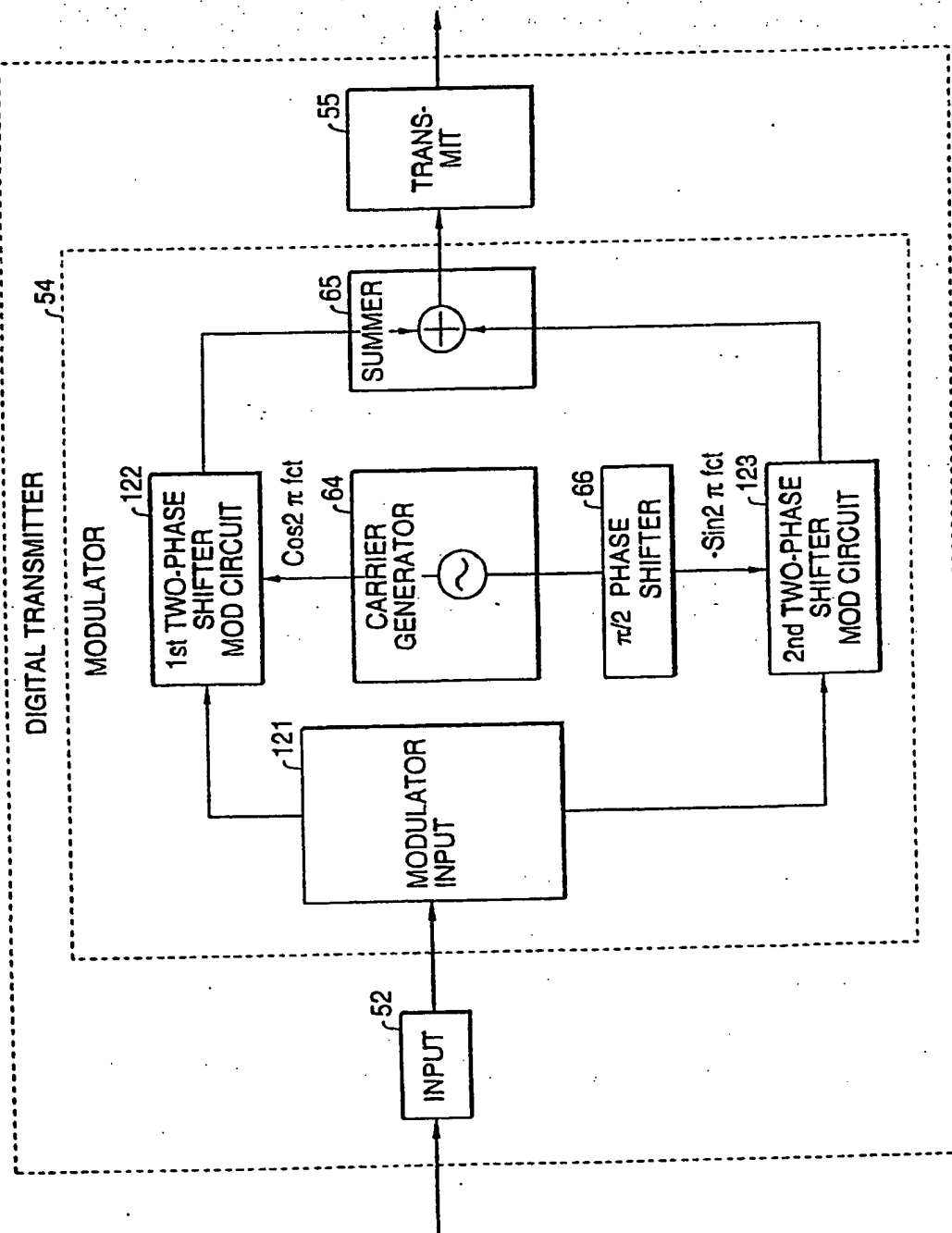
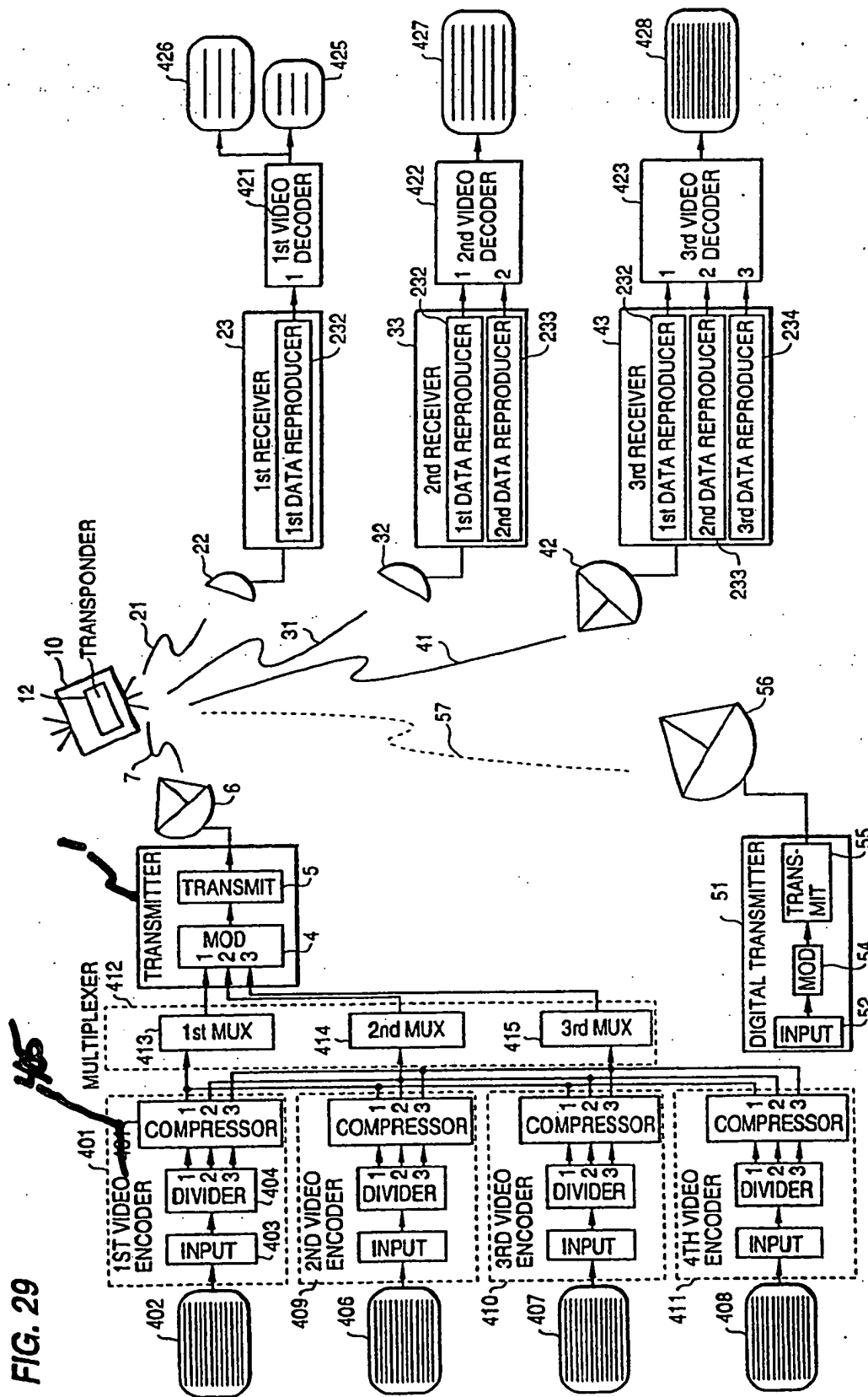


FIG. 17



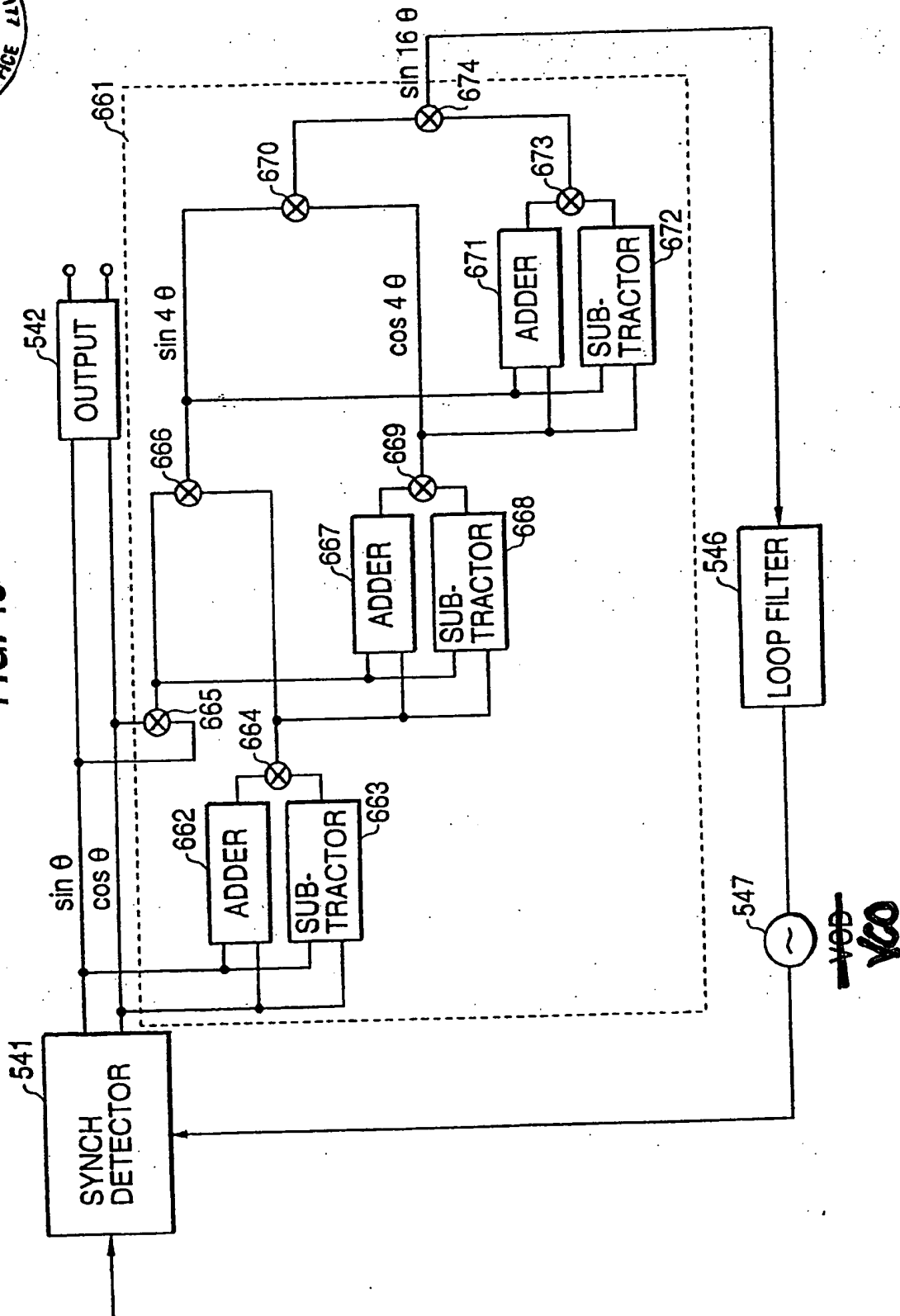




FIG. 65

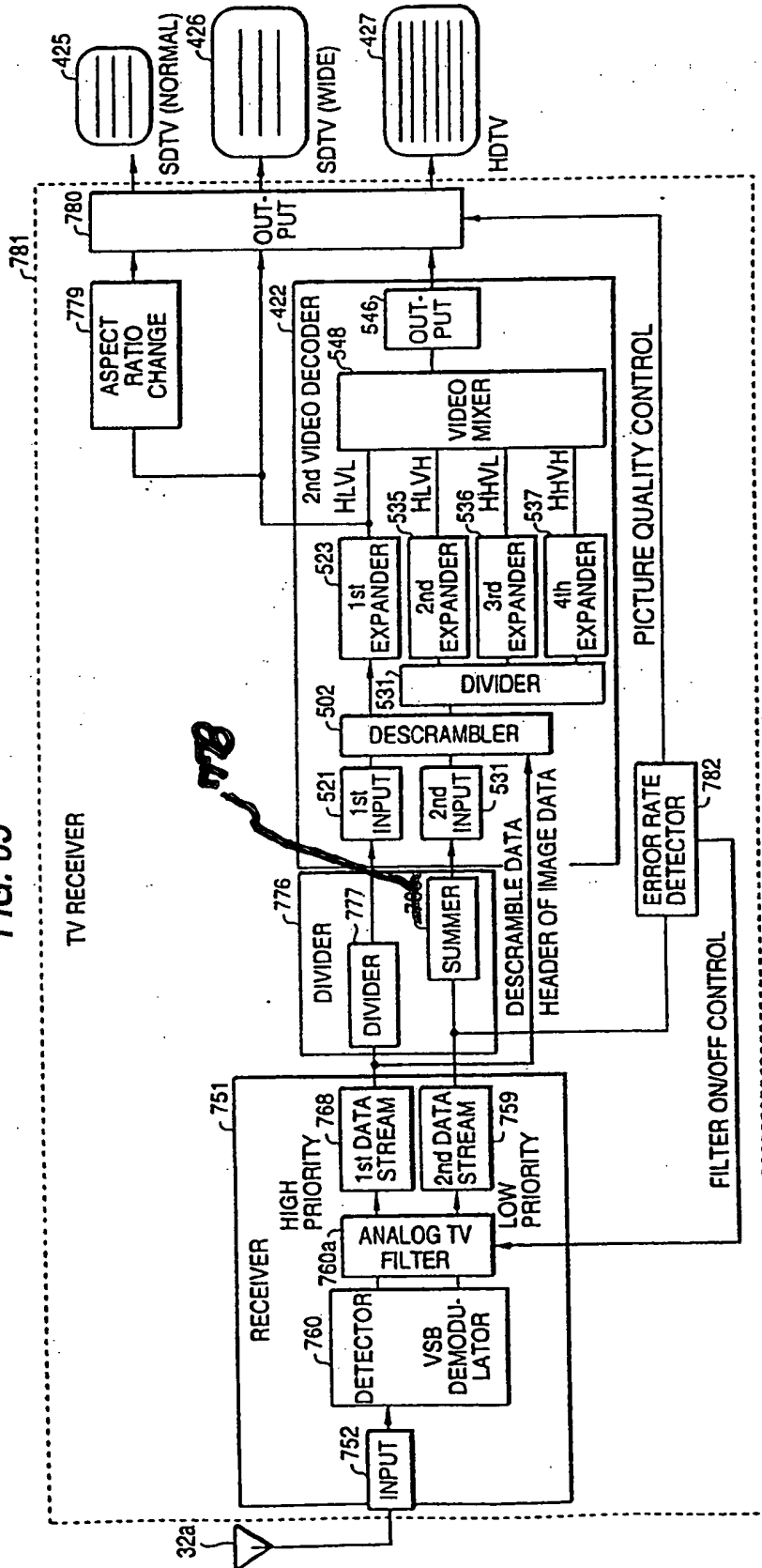




FIG. 67

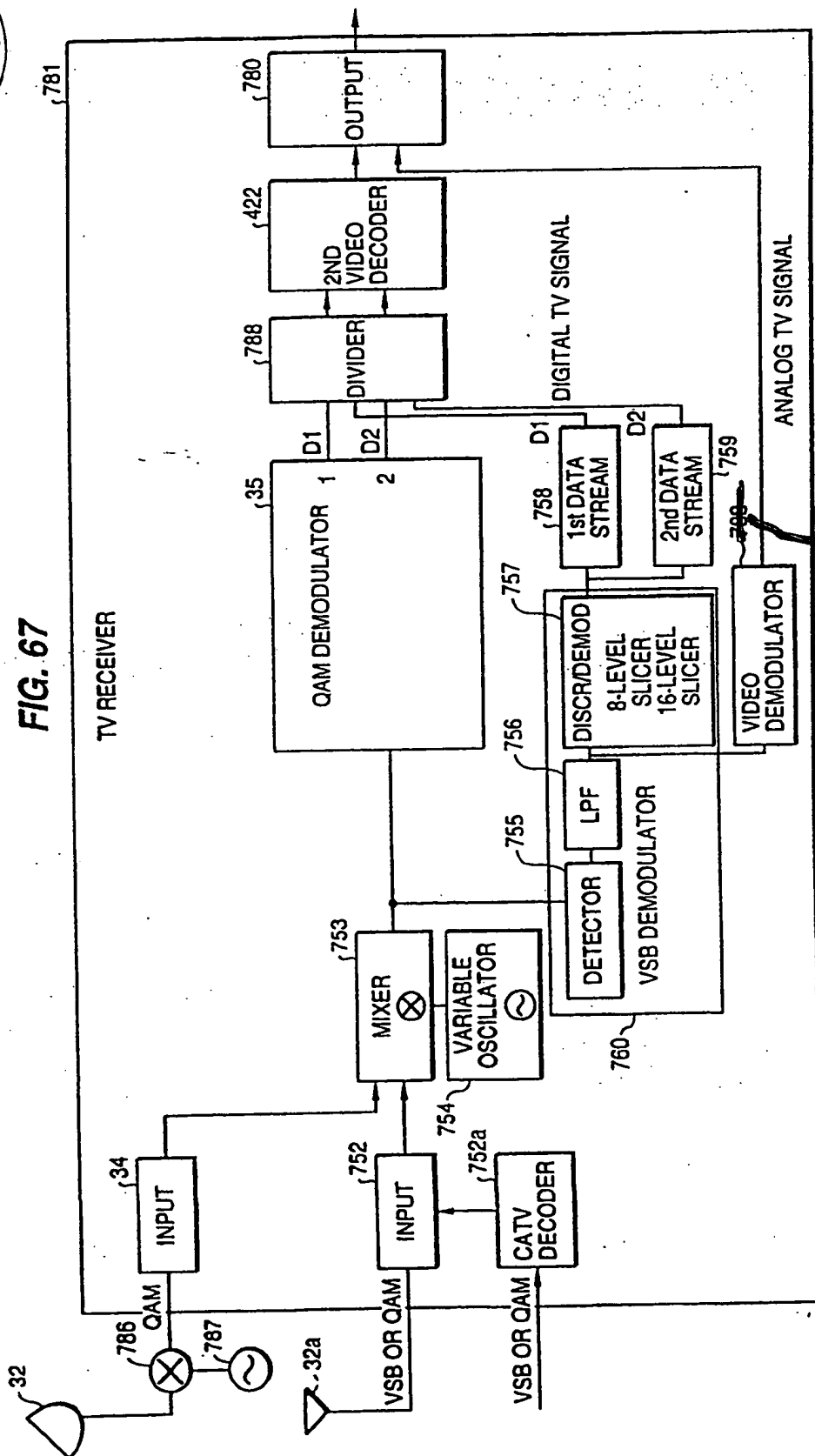






FIG. 93

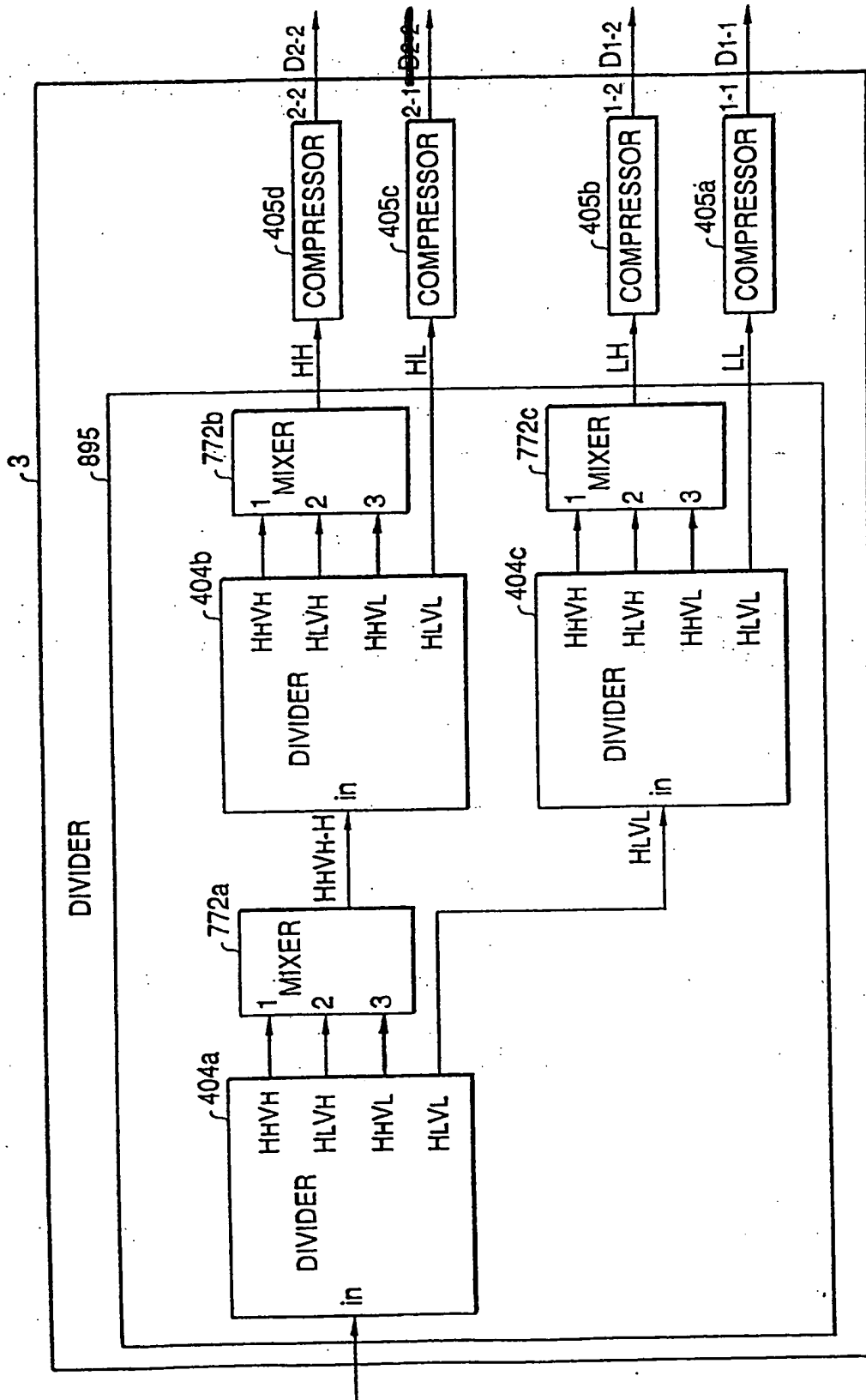
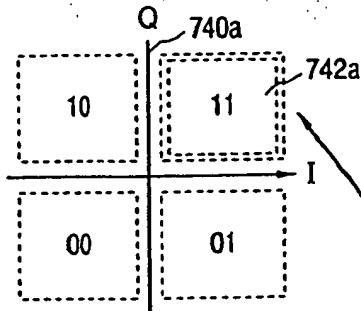


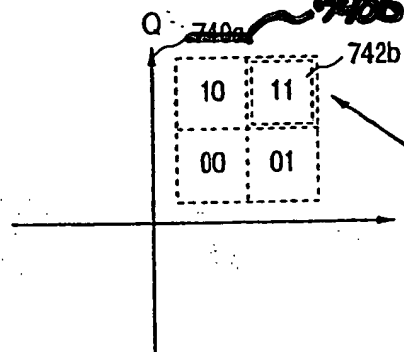


FIG. 112

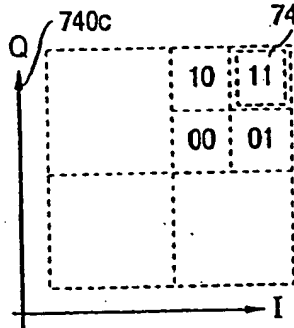
SUBCHANNEL-1 (SRQAM:D1 = 2bit)



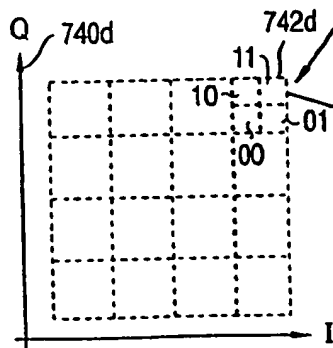
SUBCHANNEL-2 (16-SRQAM:D2 = 2bit)



SUBCHANNEL-3 (64-SRQAM:D3 = 2bit)



SUBCHANNEL-4 (256-SRQAM:D4 = 2bit)



CODE WORD-1

CODE WORD-2

CODE WORD-3

CODE WORD-4

741a 11 2bit

741b 11 2bit

741c 11 2bit

741d 11 2bit

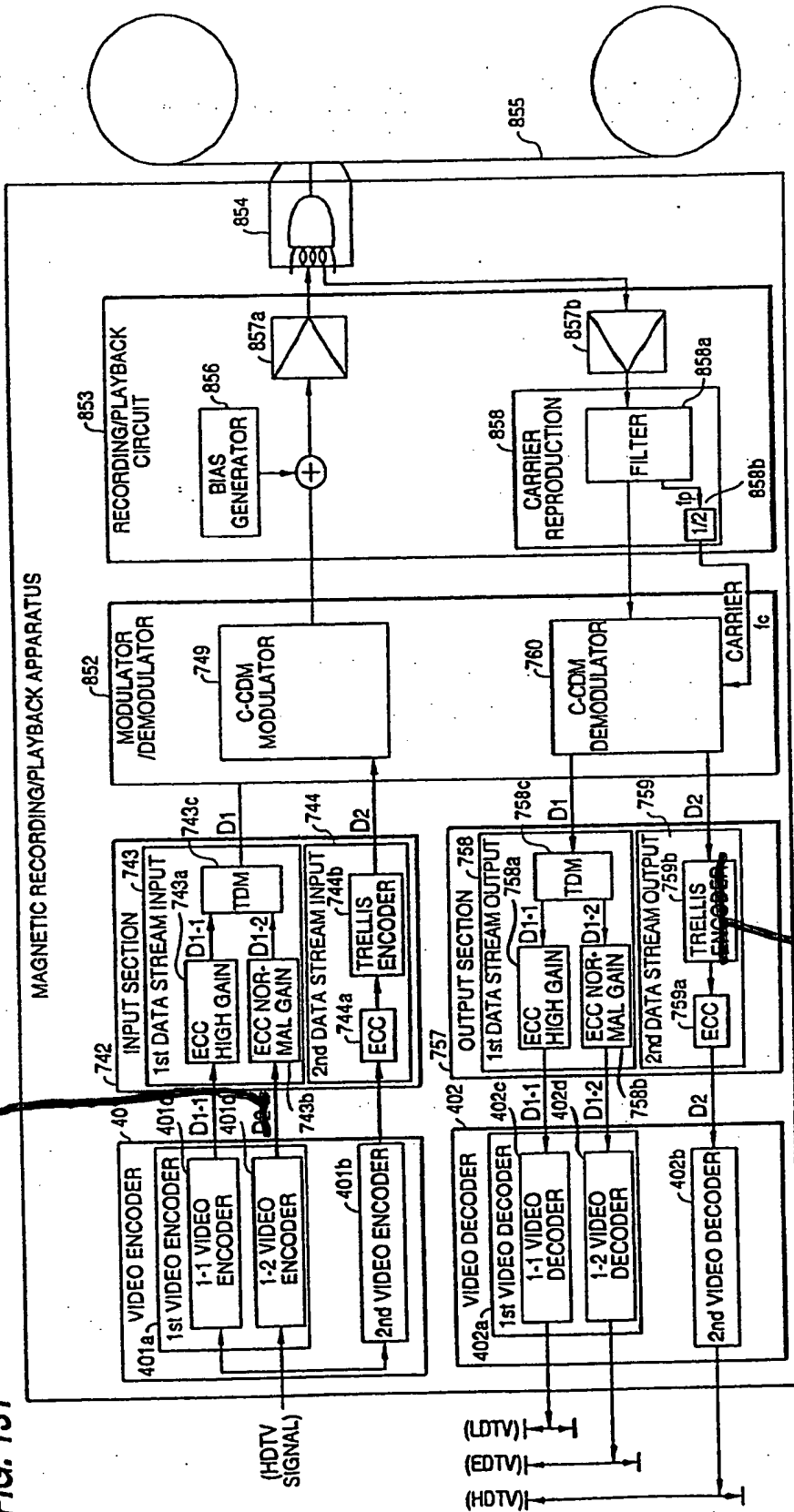
8bit

SIGNAL POINT  
CODE WORD  
11 11 11 11



*Dra*

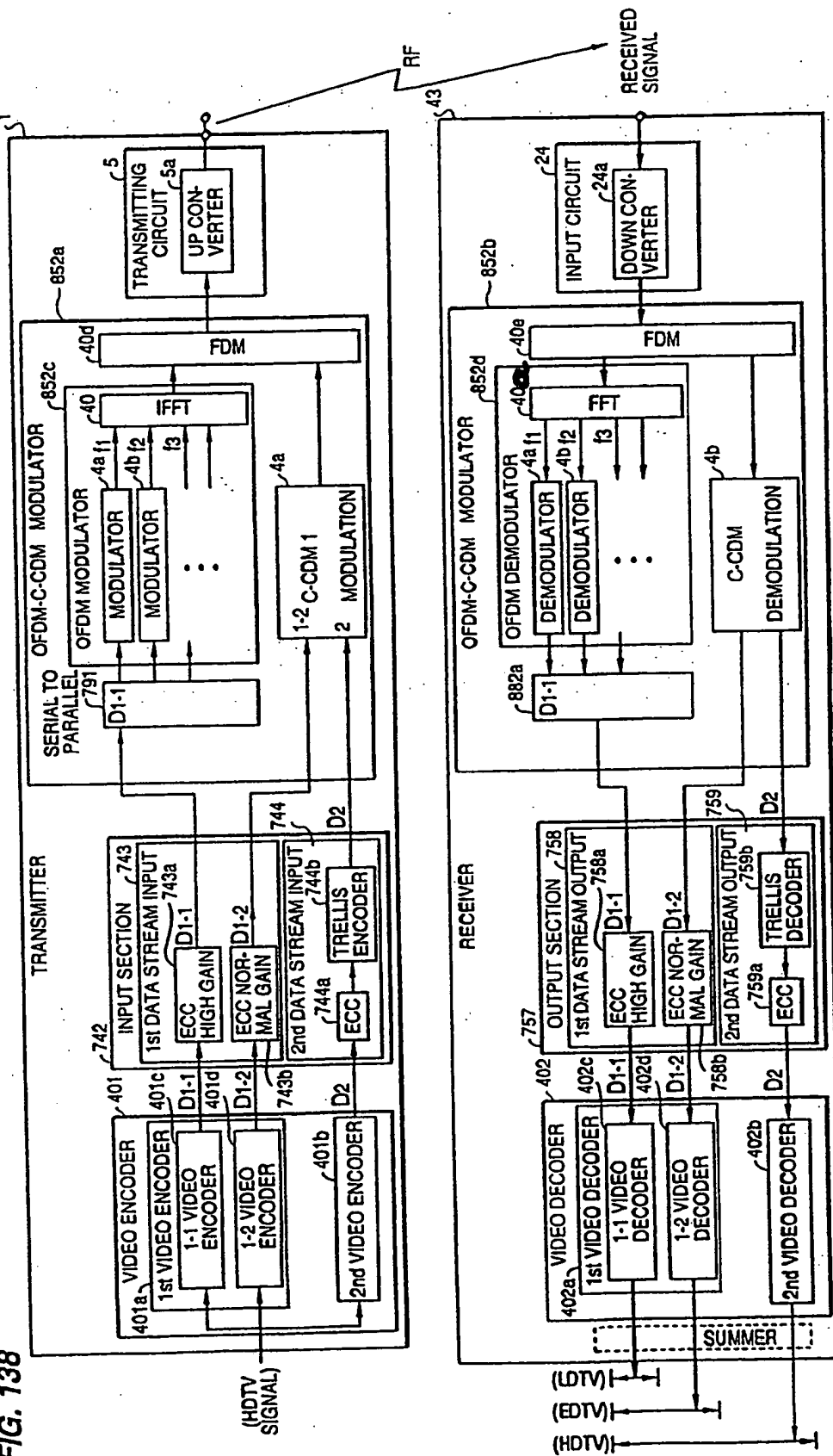
FIG. 131



*Decoder*



FIG. 138



The diagram illustrates a video transmission system with a transmitter and a receiver. The transmitter path (left) starts with an HDTV signal, which is processed by a video encoder (401a, 401b) and then a weighted OFDM modulator (791). The receiver path (right) starts with a received signal, which is processed by a weighted OFDM demodulator (852a, 852b) and then a video decoder (402a, 402b). Both paths include serial-to-parallel and parallel-to-serial converters (791a, 791b) and a summer (43) for combining signals. The transmitter path also includes an input section (743) and an output section (758) for data stream processing.

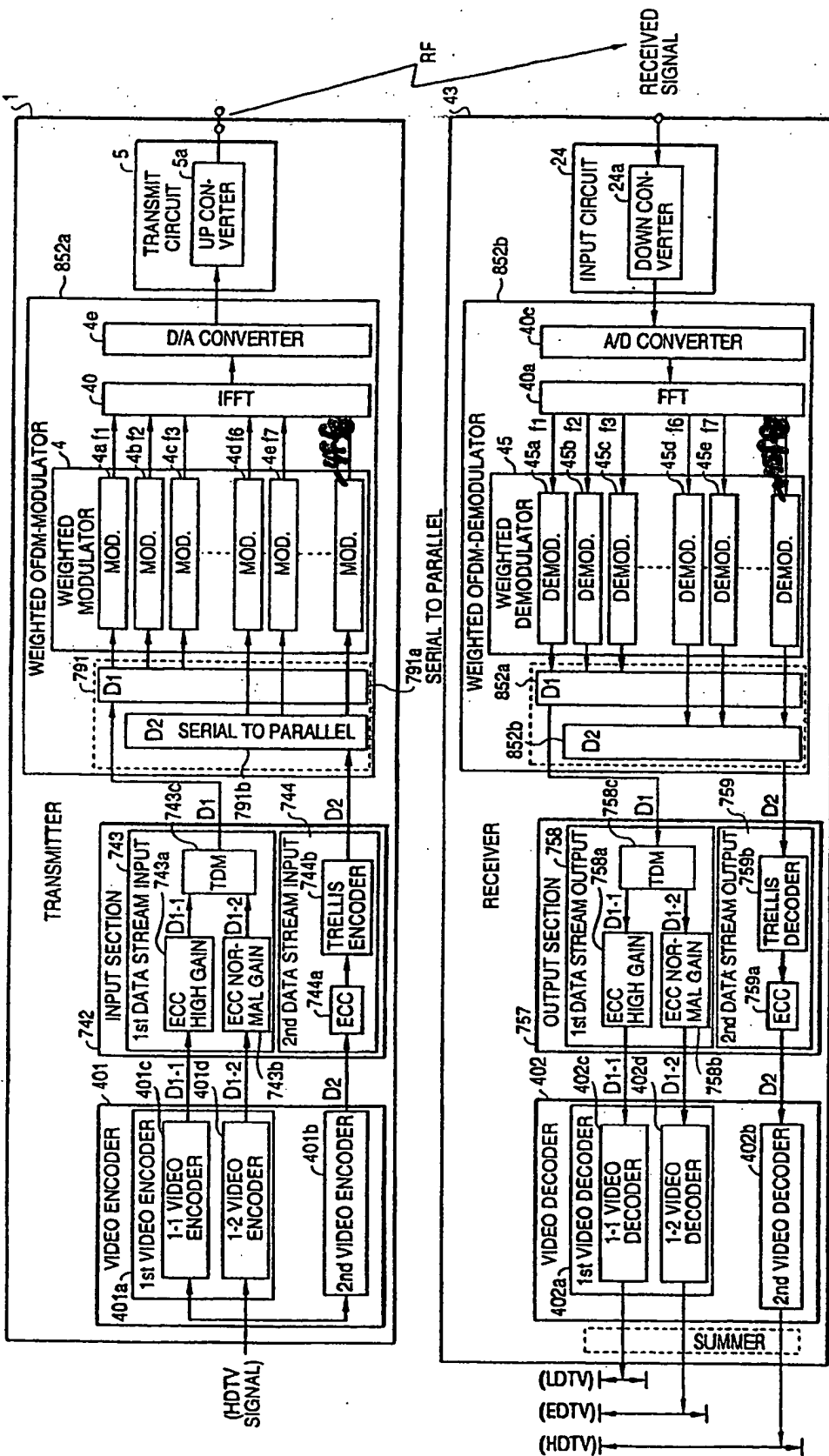


FIG. 169

